



501.39619X00/219900825US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: SHIMODA, et al.

Serial No.: 09/783,604

Filed: February 15, 2001

For: METHOD FOR ANALYZING CIRCUIT PATTERN DEFECTS
AND A SYSTEM THEREOF

Group: 2623

Examiner: V. Kibler

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 5, 2005

Sir:

In response to the Office Action dated 05 April 2005, please amend the
above-identified application as listed below and as set forth on the following pages:

Amendments to the Claims

Remarks are included following the amendments